CLAIM AMENDMENTS:

Claim 1 (Canceled).

Claim 2 (Canceled).

Claims 3 and 4 (Canceled).

Claim 5 (Currently amended): A combined semiconductor apparatus, comprising:

a silicon substrate having an integrated circuit formed therein, the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit;

a planarized region defined over said rough or irregular surface of said silicon substrate;

a substantially planar metal layer disposed over said planarized region; and

[[a]] at least one semiconductor thin film which is made from other process, disposed over said metal layer, [[the]] each semiconductor thin film being made to be small enough to include ~~including~~ a single light-emitting element and being bonded on said metal layer, so that said each semiconductor thin film is disposed above the integrated circuit and said metal layer electrically connects said light-emitting element to said integrated circuit, said semiconductor thin film

being made of an inorganic compound semiconductor as a main material~~, said semiconductor thin film being disposed so as not to extend outward from edges of the metal layer~~.

Claim 6 (Previously presented): The combined semiconductor apparatus according to claim 39, wherein said planarized film includes an interdielectric layer.

Claims 7 and 8 (Canceled).

Claim 9 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said semiconductor thin film has a common electrode layer on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor thin film, in which said light-emitting element is formed, and

said second surface of said semiconductor thin film is disposed on a side of said planarized region of said silicon substrate.

Claim 10 (Previously presented): The combined semiconductor apparatus according to claim 9, wherein said integrated circuit includes individual electrode terminals; and

said apparatus further comprising individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual electrode terminal.

Claims 11- 17 (Canceled).

Claim 18 (Previously presented): The combined semiconductor apparatus according to claim 5, wherein said light-emitting element is a plurality of said light-emitting elements arranged in said semiconductor thin film.

Claim 19 (Canceled).

Claim 20 (Previously presented): An optical print head including the combined semiconductor apparatus of claim 5.

Claims 21-36 (Canceled).

Claim 37 (Previously presented): The combined semiconductor apparatus according to claim 5, further comprising an interdielectric layer formed in a region peripheral to said metal layer between the planarized region and the semiconductor thin film, wherein the interdielectric layer has the same thickness

as that of the metal layer, and the metal layer and the interdielectric layer collectively form a planarized film.

Claim 38 (Canceled).

Claim 39 (Previously presented) The combined semiconductor apparatus according to claim 5, further comprising a planarized film disposed on said planarized region, wherein said metal layer is disposed on said planarized film.

Claim 40 (New) The combined semiconductor apparatus according to claim 5, wherein said main material is a material selected from the group consisting of $(Al_xGa_{1-x})_yIn_{1-y}P$, where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, GaN, AlGaN, InGaN, GaAs and AlGaAs.

Claim 41 (New) The combined semiconductor apparatus according to claim 5, wherein said light-emitting element is in direct contact with said metal layer.

Claim 42 (New) A method of fabricating a combined semiconductor apparatus, comprising:

forming a silicon substrate having an integrated circuit formed therein, the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit;

forming a planarized region defined over said rough or irregular surface of said silicon substrate;

forming a substantially planar metal layer disposed over said planarized region; and

forming at least one semiconductor thin film to be small enough to include a single light-emitting element;

after forming each semiconductor thin film with the light-emitting element, disposing each semiconductor thin film over said metal layer, and bonding said each semiconductor thin film on said metal layer, so that said light-emitting element is in contact with said metal layer, said each semiconductor thin film is disposed above the integrated circuit, and said metal layer electrically connects said light-emitting element to said integrated circuit, said semiconductor thin film being made of an inorganic compound semiconductor as a main material.